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IN THE U.S. PATENT AND TRADEMARK OFFICE

In re Application of

Gerard Chauvel, et al.

Serial No.: 08/890,894

Filed: 07/10/97

TIF-15767A

Examiner: D. Tran

Art Unit: 2186

For: MULTIPLE PROCESSOR APPARATUS HAVING A PROTOCOL PROCESSOR INTENDED FOR THE EXECUTION OF A COLLECTION OF INSTRUCTIONS IN A REDUCED NUMBER OF OPERATIONS

APPEAL BRIEF TRANSMITTAL FORM

MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8(A)

I hereby certify that on this day this correspondence is being deposited with the US Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner For Patents, Washington, DC 20231.

Elizabeth Austin — Date 1/31/01

Assistant Commissioner for Patents

Washington, DC 20231

Dear Sir:

Transmitted herewith in triplicate is a Substitute Appellant's Brief in the above-identified application.

Charge any additional fees, or credit overpayment to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. An original and two copies of this sheet are enclosed.

Respectfully submitted,

Ronald O. Neerings
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Gerard Chauvel, et al.

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SUBSTITUTE APPELLANTS' BRIEF

Assistant Commissioner for Patents
Washington, D.C. 20231

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Elizabeth Austin — Date 1/31/02

Dear Sir:

In support of their appeal of the Final Rejection of claims in the above-referenced application and in response to the Notification of Non-Compliance with 37 CFR 1.192(c) mailed on January 17, 2001, Appellants respectfully submit herein their Substitute Brief and Substitute Appendix (attached hereto).

I. REAL PARTY IN INTEREST

Texas Instruments Incorporated is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals or interferences.

III. STATUS OF CLAIMS

Claims 6-15, 17, 19, and 34-39 are pending in the application. Final Rejection of Claims 6-15, 17, 19, and 34-39 was made by the Examiner in the Office Action dated January 19, 2000. Claims 6-15, 17, 19, and 34-39 are on appeal. Claims 6-15, 17, 19, and 34-39 are reproduced in the Appendix to Appellants' Brief filed herewith.

IV. STATUS OF AMENDMENTS

Appellants filed an amendment under 37 C.F.R. 1.116 on June 27, 2000, in response to the final rejection of January 19, 2000. In the Advisory Action dated July 28, 2000, the Examiner indicated that the proposed amendment will be entered upon the filing of this appeal.

V. SUMMARY OF THE INVENTION

One embodiment of the invention comprises: a first processor (6) for performing scalar processing, said first processor comprising a core (9), a program memory (13) and a local memory (14); a second processor (5) for performing vector processing, said second processor comprising a core (8), a program memory (11) and a local memory (12); a synchronizing circuit (10) for coupling said core of said first processor to said core of said second processor; and a memory circuit (15) for coupling said local memory of said first processor to said local memory of said second processor (see Figure 5; page 1, lines 7-22; page 5, line 31 - page 6, line 7; page 6, lines 23-26).

Another embodiment of the invention comprises: a first processor (5) comprising a core (8), a program memory (11) and a local memory (12); a second processor (6) comprising a core (9), a program memory (13) and a local memory (14); a synchronizing circuit (10) for coupling said core of said first processor to said core of said second processor; and one and only one common memory (10) coupling said local memory of said first processor to said local memory of said second processor (see Figure 5; page 5, line 31 - page 6, line 7; page 6, lines 23-26).

Still another embodiment of the invention comprises: a main processor (5) comprising a core (8), a program memory (11) and a local memory (12); a protocol processor (6) comprising a core (9), a program memory (13) and a local memory (14); a synchronizing circuit (10) for coupling said core of said main processor to said core of said protocol processor; and one and only one common memory (15) coupling said local memory of said main processor to said local memory of said protocol processor (see Figure 5; page 5, line 31 - page 6, line 7; page 6, lines 23-26).

Yet another embodiment of the invention comprises: a main processor (5) comprising a core (8), a program memory (11) and a local memory (12); a protocol processor (6) comprising a core (9), a program memory (13) and a local memory (14), said protocol processor being suited to execute tasks to which the main processor is not suited; a synchronizing circuit (10) for coupling said core of said main processor to said core of said protocol processor; and a common memory (15) coupling said local memory of said main processor to said local memory of said protocol processor (see Figure 5; page 2, lines 6-15; page 5, line 31 - page 6, line 7; page 6, lines 23-26).

Still yet another embodiment of the invention comprises: a main processor (5) comprising a core (8), a program memory (11) and a local memory (12); a protocol processor (6) comprising a core (9), a program memory (13) and a local memory (14), said protocol processor being suited to execute tasks to which the main processor is not suited; a synchronizing circuit (10) for coupling said core of said main processor to said core of said protocol processor; and one and only one common memory (15) coupling said local memory of said main processor to said local memory of said protocol processor (see Figure 5; page 2, lines 6-15; page 5, line 31 - page 6, line 7; page 6, lines 23-26).

VI. ISSUES

1) Are Claims 6, 14-15 and 17 patentable under 35 U.S.C. 102(e) over Aoyama et al., U.S. Patent No. 4,964,035?

2) Are Claims 8-13, 19 and 34-35 patentable under 35 U.S.C. 103(a) over Aoyama et al., U.S. Patent No. 4,964,035?

3) Are Claims 36-39 patentable under 35 U.S.C. 103(a) over Aoyama as applied to claim 6 above, and further in view of Ngai et al., EP 0 157 306 A3?

4) Is Claim 7 patentable under 35 U.S.C. 103(a) over Aoyama as applied to claim 6 above, and further in view of Ngai et al., EP 0157 306 A3?

VII. GROUPING OF CLAIMS

Claims 6-15, 17, 19 and 34-39 stand separately.

VIII. ARGUMENT

The Rejection

Claims 6, 15-15 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Aoyama et al., U.S. Patent No. 4964035, (herein Aoyama).

As per claim 6, Aoyama teaches the claimed invention, comprising: a first processor for performing scalar processing (e.g., fig. 1, el. 600), comprising a core, a local memory, and a program memory (e.g., fig. 1, els. 601 and 602; and col. 5, lines 47 et seq.); a second processor for

performing vector processing (e.g., fig. 1, el. 500, vector processor), comprising a core, a local memory and a program memory (e.g., fig. 1, els. 501 and 502; and col. 8, lines 4 et seq.); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig. 1, els 810 or 800a, cols. 5-6); and a memory circuit for coupling the local memory of the first processor to local memory of the second processor (e.g., fig. 1, el. 800).

As per claim 14, 15, and 17, Aoyama teaches the memory circuit coupling between the first and second processors being physically separate from the first and second processors (e.g., fig. 1, el. 800); the memory circuit being DPRAM memory (e.g., col. 10); and the synchronizing circuit ensure that only one of the processors utilized the memory circuit at any one time (e.g., cols. 5-6).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama as applied to claim 6 above, and further in view of Ngai et al., EP 0 157 306 A3, (hereinafter Ngai).

As per claim 7, Aoyama does not explicitly show the use of the second processor being a main processor. Ngai show the use of a main processor (e.g., abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Ngai into the Aoyama's system because it would provide for improving system performance by having a vector processor being a main processor to perform complex functions for the vector processor system.

Claims 8-13, 19 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al., U.S. Patent No. 4,964,035, (herein after Aoyama).

As per claim 8, Aoyama does not specifically show the scalar processor as a microprocessor. "Official Notice" is taken that both the concept and advantages of providing for the incorporation of a scalar processor into a microprocessor are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the incorporation of a processor into a microprocessor to Aoyama because it would

provide for a reduction in chip space and signal lines between functional elements, leading to an increase in processing performance.

As per claim 9, Aoyama does not specifically show the second processor as a DSP. "Official Notice" is taken that both the concept and advantages of providing DSP to perform in signal processing in the vector processing system are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a DSP into the vector processing system of Aoyama because it would provide for an increase in functionality in performing signal processing tasks.

As per claims 10-13, Aoyama does not specifically show the local memories as RAM; the program memory as a ROM; and the second processor comprising a ROM coupled to an incrementation register. "Official Notice" is taken that both the concept and advantages of providing a local memory as RAM; a program memory as ROM; and a ROM coupled to an incrementation register are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to includes RAMS; ROMs; and a ROM coupled to an incrementation register into the vector processing system of Aoyama because it would allow a storage location to be read and written in any order; a storage system to not loose data when power is removed from it; and stepping through a program memory in the second memory.

As per claim 19, Aoyama shows the use of providing an instruction set to the first processor, comprising at least one field of execution conditions and classes of instructions: transfer operations between the memory and a register in the scalar processor, and monitoring scalar processing operations (e.g. col. 1-2). Aoyama does not explicitly shows a transfer operations between a protocol processor and memory; and monitoring of all the operations modifying the value of an incrementation register in a protocol processor. "Official Notice" is taken that both the concept and advantages of providing integer instructions corresponding to ALU operations on integer numbers; providing a protocol processor in a vector-scalar processing system; and an incrementation register is well known and expected in the art. It would have been obvious to one of

ordinary skill in the art to include an integer instructions corresponding to ALU operations on integer numbers; providing a protocol processor with a register for transferring data; and an incrementation register in a protocol processor into Aoyama because it would allow the system to increase functionality by performing integer operations; and performing scalar processing high level tasks in the system.

As per claims 34-35, Aoyama teaches the vector processor and matrix computations; and the scalar processor (e.g., fig. 1., els 500 and 600 and cols. 1-2), but does not explicitly show the use of scalar processing encompassed a high level task which is the monitoring of an application or the management of functioning and tasks which are generally carry out by hard-wired logic which are the protocol processing; and vector processing including signal processing tasks generally carrying out by a DSP and the use of array processor type. "Official Notice" is taken that both the concept and advantages of providing integer instructions corresponding to ALU operations on integer numbers; providing scalar processing encompassed a high level task which is the monitoring of an application or the management of functioning and tasks which are generally carry out by hard-wired logic which are the protocol processing; and vector processing including signal processing tasks generally carrying out by a DSP and the use of array processor type are well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include a protocol processor; and DSP and array processor into Aoyama because it would allow scalar processing to encompass high level tasks; and signal processing and matrix computations to be performed.

Claims 36-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama as applied to claim 6 above, and further in view of Ngai et al., EP 0 157 306 A3, (hereinafter Ngai).

As per claims 36-39, Aoyama teaches the invention substantially as claimed, comprising: a first processor for performing scalar processing (e.g., fig. 1, el. 600), comprising a core, a local memory, and a program memory (e.g., fig. 1, els. 601 and 602; and col. 5, lines 47 et seq.), where the first processor being suited to execute tasks to which the main processor is not suited; a second processor for performing vector processing (e.g., fig. 1, el. 500, vector processor), comprising a core, a local memory and a program memory (e.g., fig. 1, els. 501 and 502; and col. 8, lines 4 et

seq.); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig. 1, els 810 or 800a, cols. 5-6); and one and only one common memory circuit for coupling the core of the first processor to the core of the second processor (e.g., fig. 1, els 810 or 800a, cols. 5-6); and one and only one common memory circuit for coupling the local memory of the first processor to local memory of the second processor (e.g., fig. 1, el. 800). Aoyama does not explicitly show the use of the second processor being a main processor. Ngai show the use of a main processor (e.g., abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Ngai into the Aoyama's system because it would provide for improving system performance by having a main processor to perform complex operations for the vector processing system. Aoyama does not explicitly shown the use of the first processor being a protocol processor. "Official Notice" is taken that both the concept and advantages of providing a protocol processor to a vector-scalar processing system are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a protocol processor to the system of Aoyama because it would allow the system to encompass scalar processing high level tasks.

APPELLANT'S ARGUMENT

1) Claims 6, 14-15 and 17 are patentable under 35 U.S.C. 102(e) over Aoyama et al., U.S. Patent No. 4,964,035.

35 U.S.C. 102(b) requires that a person shall be entitled to a patent unless the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent. Case law holds that "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Unior Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Independent Claim 6, as amended, requires and positively recites, "a first processor for performing scalar processing, said first processor comprising a core, **a program memory and a local memory**", "a second processor for performing vector processing, said second processor comprising a core, **a program memory and a local memory**", "a synchronizing circuit for coupling said core of said first processor to said core of said second processor" and "a memory circuit **for coupling said local memory of said first processor to said local memory of said second processor**".

The Examiner states that Aoyama teaches the claimed invention, comprising: a first processor for performing scalar processing (e.g., fig. 1, el. 600), comprising a core, a local memory, and a program memory (e.g., fig. 1, els. 601 and 602; and col. 5, lines 47 et seq.); a second processor for performing vector processing (e.g., fig. 1, el. 500, vector processor), comprising a core, a local memory and a program memory (e.g., fig. 1, els. 501 and 502; and col. 8, lines 4 et seq.); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig. 1, els 810 or 800a, col. 5-6); and a memory circuit for coupling the local memory of the first processor to local memory of the second processor (e.g., fig. 1, el. 800)(Office Action dated 1/19/00, page 5, line 17 page 6, line 6). Applicants respectfully traverse.

The Aoyama reference discloses a device in which the vector processor comprises a vector register 502 coupling vector arithmetic 501 to address translation 503. Address translation 503 is coupled to main storage 700 (which is external to vector processor (VP)). Accordingly, since main storage 700 is not part of vector processor (VP), it is not an "on-board" local memory or program memory that is part of vector processor (VP). The Examiner relies upon col. 8, lines 4 et seq. to support her argument that Aoyama's vector processor contains both a **program memory and a local memory**. The Examiner is obviously relying upon main storage (MS) 1 as being one of the program memory or local memory - e.g., the teaching that "an address generated by the vector instruction address generate circuit 200 is sent to the main storage 1, and a vector instruction read from the main storage 1 is sent to a register 201" (col. 8, lines 12-15). Unfortunately, the Examiner's reliance on Aoyama is misplaced. Aoyama discloses that "the address generate circuit 200 is configured in the same fashion as the scalar instruction read circuit of FIG. 4 (col. 8, lines 9-

12). Aoyama further discloses that MS 1 corresponds to main storage 700 in FIG. 1 (col. 5, lines 31-32). Main storage 700 is NOT part of vector processor 500 or scalar processor 600. Accordingly, Aoyama fails to teach or suggest, "a second processor for performing vector processing, said second processor comprising a core, **a program memory and a local memory**", as is required by Claim 6. Moreover, vector processor (VP) has no equivalent to buffer storage 602 of scalar processor 600, which the Examiner relies upon as one of the memories for scalar processor 600. As a result, the 35 U.S.C. 102(e) rejection of Claim 6 is improper.

Claim 14 further defines the apparatus of Claim 6, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second processor is physically separate from said first and second processors. In addition to the reasons submitted above for the allowance of Claim 6 (upon which Claim 14 depends) over Aoyama, Appellants respectfully submit that reference to figure 1 clearly shows that it is control logic 810 that couples the first and second processors - NOT common memory 800. As a result, the Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 15 further defines the apparatus of Claim 6, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second processor is a DPRAM memory. The Examiner states that Aoyama discloses a DPRAM on col. 10. Appellants respectfully disagree. In addition to the reasons submitted above for the allowance of Claim 6 (upon which Claim 15 depends) over Aoyama, Appellants respectfully point out that Column 10 of Aoyama discloses random access memories RAMs 108_1, 108_2, 108_3 (col. 10, lines 13-18) - NOT a DPRAM. Accordingly, the Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 17 further defines the apparatus of Claim 6, wherein said synchronizing circuit ensures that only one of said first and processors utilizes said memory circuit for coupling said local memory of said first processor to said local memory of said second processor, at any one time. In addition to the reasons submitted above for the allowance of Claim 6 (upon which Claim 17 depends) over Aoyama, Appellants respectfully submit that since Aoyama does not disclose

separate local memories for the first and second processors, it cannot teach a "synchronizing circuit ensures that only one of said first and processors utilizes said memory circuit for coupling said local memory of said first processor to said local memory of said second processor, at any one time". Accordingly, the Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

2) Claims 8-13, 19 and 34-35 are patentable under 35 U.S.C. 103(a) over Aoyama et al., U.S. Patent No. 4,964,035.

Claim 8 further defines the apparatus of Claim 7, wherein said first processor is a microprocessor. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 7. In addition to the previously identified deficiency of Aoyama as applied to Claims 6 and 7, Applicants traverse the Examiner's stated Official Notice that "both the concept and advantages of providing for the incorporation of a scalar processor into a microprocessor are well known and expected in the art" and "it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the incorporation of a processor into a microprocessor to Aoyama because it would provide for a reduction in chip space and signal lines between functional element, leading to an increase in processing performance" (Office Action dated 01/19/00, page 7, lines 13-18). Applicants respectfully submit that the "level of skill in the art" is the level "at the time of the invention - June 1991", not the present level of skill in the art. The Examiner has provided no pre-June 1991 motivation in the art for such a modification. The Examiner's obviousness rational is improper hindsight reconstruction.

Claim 9 further defines the apparatus of Claim 7, wherein said second processor is a digital signal processor "DSP". The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 7. The Examiner readily admits that Aoyama does not show the second processor as a DSP (Office Action dated 01/19/00, page 8, line 1). Further, in addition to the previously identified deficiency of Aoyama as applied to Claims 6 and 7, Applicants traverse the Examiner's stated Official Notice that "both the concept and advantages of providing

DSP to perform signal processing in the vector processing system are well known and expected in the art" and "it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a DSP into the vector processing system of Aoyama because it would provide for an increase in functionality in performing signal processing tasks (Office Action dated 01/19/00, page 8, lines 13-18). Applicants respectfully submit that the "level of skill in the art" is the level "at the time of the invention - June 1991", not the present level of skill in the art. The Examiner has provided no pre-June 1991 motivation in the art for such a modification. The Examiner's obviousness rational is improper hindsight reconstruction.

Claim 10 further defines the apparatus of Claim 6, wherein said program memory of said first processor is ROM memory. The Examiner readily admits that Aoyama does not show that the program memory of said first processor is ROM memory (Office Action dated 01/19/00, page 8, lines 7-8). The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of allowable Claim 6. Accordingly, Claim 10 is allowable. The Examiner's rationale for obviating the claim is nothing more than hindsight reconstruction.

Claim 11 further defines the apparatus of Claim 6, wherein said local memory of said first processor is RAM memory. The Examiner readily admits that Aoyama does not show that the local memory of the first processor is RAM memory (Office Action dated 01/19/00, page 8, lines 7-8). The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6. Accordingly, Claim 11 is allowable. The Examiner's rationale for obviating the claim is nothing more than hindsight reconstruction.

Claim 12 further defines the apparatus of Claim 6, wherein said program memory of said second processor is ROM memory. The Examiner readily admits that Aoyama does not show that the local memory of the first processor is RAM memory (Office Action dated 01/19/00, page 8, lines 7-8). The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6. Accordingly, Claim 12 is allowable. The Examiner's rationale for obviating the claim is nothing more than hindsight reconstruction.

Claim 13 further defines the apparatus of Claim 6, wherein said local memory of said second processor is RAM memory. The Examiner readily admits that Aoyama does not show that the local memory of the first processor is RAM memory (Office Action dated 01/19/00, page 8, lines 7-8). The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6. Accordingly, Claim 13 is allowable. The Examiner's rationale for obviating the claim is nothing more than hindsight reconstruction.

Claim 19 further defines the apparatus of Claim 6, wherein an instruction set is provided to said first processor, comprising at least one field of execution conditions which is intended therefor and comprises at least the following classes of instructions: integers corresponding to arithmetic and logic operations on integer numbers; transfer corresponding to the transfer operations between a register in said protocol processor and memory; and monitoring corresponding to the monitoring of all of the operations modifying the value of an incrementation register in said protocol processor. Applicants traverse the Examiner's stated Official Notice that "both the concept and advantages of providing a protocol processor in a vector-scalar processing system; and an incrementation register is well known in the art" and "it would have been obvious to one of ordinary skill in the art at the time the invention was made to include an integer instructions corresponding to ALU operations on integer numbers; providing a protocol processor with a register for transferring data; and an incrementation register in a protocol processor into Aoyama because it would allow the system to increase functionality by performing integer operations; and performing scalar processing high level tasks in the system (Office Action dated 01/19/00, page 9, lines 8-16). Applicants respectfully submit that the "level of skill in the art" is the level "at the time of the invention - June 1991", not the present level of skill in the art. The Examiner is obviously relying upon present day motivation and has provided no pre-June 1991 motivation in the art for such a modification. The Examiner's obviousness rational is improper hindsight reconstruction.

Claim 34 further defines the apparatus of Claim 6, wherein said scalar processing encompasses a high-level task which is the monitoring of an application or the management of functioning and tasks which are generally carried out by hard-wired logic which are the protocol processing. The Aoyama reference fails to teach or suggest this further limitation in combination

with the requirements of Claim 6. In addition to the previously identified deficiency of Aoyama as applied to Claim 6, Applicants traverse the Examiner's stated Official Notice that "both the concept and advantages of providing integer instructions corresponding to ALU operations on integer numbers; providing scalar processing encompassed a high level task which is the monitoring of an application or the management of functioning and task which are generally carry out by hard-wired logic which are the protocol processing; and vector processing including signal processing tasks generally carrying out by a DSP and the use of array processor type are well known and expected in the art - it would have been obvious to one or ordinary skill in the art to include a protocol processor; and DSP and array processor into Aoyama because it would allow scalar processing to encompass high level teaks; and signal processing and matrix computations to be performed (Office Action dated 01/19/00, page 10, lines 3-11). Appellants respectfully submit that the "level of skill in the art" is the level "at the time of the invention - June 1991", not the present level of skill in the art. The Examiner has improperly relied upon the present day teaching of the art and has provided no pre-June 1991 motivation in the art for such a modification.

Claim 35 further defines the apparatus of Claim 6, wherein said vector processing includes signal processing tasks generally carried out by a DSP and a matrix computation which requires a more powerful structure than that of the DSP and which is generally of the array processor type. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6. In addition to the previously identified deficiency of Aoyama as applied to Claim 6, Applicants traverse the Examiner's stated Official Notice that "both the concept and advantages of providing integer instructions corresponding to ALU operations on integer numbers; providing scalar processing encompassed a high level task which is the monitoring of an application or the management of functioning and task which are generally carry out by hard-wired logic which are the protocol processing; and vector processing including signal processing tasks generally carrying out by a DSP and the use of array processor type are well known and expected in the art - it would have been obvious to one of ordinary skill in the art to include a protocol processor; and DSP and array processor into Aoyama because it would allow scalar processing to encompass high level teaks; and signal processing and matrix computations to be performed (Office Action dated 01/19/00, page 10, lines 3-11). Appellants respectfully submit that the "level of skill

in the art" is the level "at the time of the invention - June 1991", not the present level of skill in the art. The Examiner has improperly relied upon the present day teaching of the art and has provided no pre-June 1991 motivation in the art for such a modification.

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references", In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing In re Lalu, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)). The Examiner in the present case has not met this burden.

Even if the cited art discloses components of the device in issue, case law holds that it is insufficient that the prior art discloses the components of the device in issue, either separately or used in other combination; there must be some teaching, suggestion, or incentive to make the combination made by the inventor. Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 934, 15 USPQ2d 1321, 1323 (Fed. Cir. 1990). Moreover, "obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Laskowski, 871 F.2d 115, 10 USPQ2d 1397 (Fed. Cir. 1989); In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984).

3) Claims 36-39 are patentable under 35 U.S.C. 103(a) over Aoyama as applied to claim 6 above, and further in view of Ngai et al., EP 0 157 306 A3.

Independent Claim 36 requires and positively recites, "a first processor comprising a core, **a program memory and a local memory**", "a second processor comprising a core, **a program memory and a local memory**", "a synchronizing circuit for coupling said core of said first processor to said core of said second processor" and "**one and only one common memory coupling said local memory of said first processor to said local memory of said second processor**".

Independent Claim 37 requires and positively recites, "a main processor comprising a core, **a program memory and a local memory**", "a protocol processor comprising a core**, a program memory and a local memory**", "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "**one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor**".

Independent Claim 38 requires and positively recites, "a **main processor** comprising a core, a program memory and a local memory", "a **protocol processor** comprising a core, a program memory and a local memory, **said protocol processor being suited to execute tasks to which the main processor is not suited**", "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "a common memory coupling said local memory of said main processor to said local memory of said protocol processor".

Independent Claim 39 requires and positively recites, "a main processor comprising a core, **a program memory and a local memory**", "a protocol processor comprising a core, **a program memory and a local memory**, said protocol processor being suited to execute tasks to which the main processor is not suited", "a synchronizing circuit for coupling said core of said first processor to said core of said second processor" and "**one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor**".

The Examiner states that Aoyama teaches the claimed invention, comprising: a first processor for performing scalar processing (e.g., fig. 1, el. 600), comprising a core, a local memory,

and a program memory (e.g., fig. 1, els. 601 and 602; and col. 5, lines 47 et seq.), wherein the first processor being suited to execute tasks to which the main processor is not suited; a second processor for performing vector processing (e.g., fig. 1, el. 500, vector processor), comprising a core, a local memory and a program memory (e.g., fig. 1, els. 501 and 502; and col. 8, lines 4 et seq.); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig. 1, els 810 or 800a, col. 5-6); and one and only one memory circuit for coupling the local memory of the first processor to local memory of the second processor (e.g., fig. 1, el. 800) (Office Action dated 1/19/00, page 10, line 15 - page 16, line 5). Applicants respectfully traverse.

The Aoyama reference discloses a device in which the vector processor comprises a vector register 502 coupling vector arithmetic 501 to address translation 503. Address translation 503 is coupled to main storage 700 (which is external to vector processor (VP)). Accordingly, since main storage 700 is not part of vector processor (VP), it is not an "on-board" local memory or program memory that is part of vector process (VP). The Examiner relies upon col. 8, lines 4 et seq. to support her argument that Aoyama's vector processor contains both a **program memory and a local memory**. The Examiner is obviously relying upon main storage (MS) 1 as being one of the program memory or local memory - e.g., the teaching that "an address generated by the vector instruction address generate circuit 200 is sent to the main storage 1, and a vector instruction read from the main storage 1 is sent to a register 201" (col. 8, lines 12-15). Unfortunately, the Examiner's reliance on Aoyama is misplaced. Aoyama discloses that "the address generate circuit 200 is configured in the same fashion as the scalar instruction read circuit of FIG. 4 (col. 8, lines 9-12). Aoyama further discloses that MS 1 corresponds to main storage 700 in FIG. 1 (col. 5, lines 31-32). Main storage 700 is NOT part of vector processor 500 or scalar processor 600. Accordingly, Aoyama fails to teach or suggest, "a second processor for performing vector processing, said second processor comprising a core, **a program memory and a local memory**", as is required by Claim 6. Moreover, vector processor (VP) has no equivalent to buffer storage 602 of scalar processor 600, which the Examiner relies upon as one of the memories for scalar processor 600.

There is no teaching or suggestion in the art that would have motivated one of ordinary skill in the art at the time of the invention to re-engineer the Aoyama device to include an internal memory, as is required by Claims 36-39, without the improper hindsight provided by Applicants' disclosure. Further, Aoyama discloses two common memories - common memory 800a and main storage (MS) 1 or 700. If the Examiner decides that both common memory 800a and main storage (MS) 1 or 700 coupled the local memory of the main processor to the local memory of the protocol processor, then Aoyama further fails to teach or suggest, "**one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor**", as is required by Claims 36, 37 and 39.

Assuming that Ngai shows the use of a main processor, as suggested by the Examiner, Appellants fail to see how adding Ngai to Aoyama overcomes the previously identified deficiencies of the Aoyama reference. Accordingly, Claims 36, 37 and 39 should be allowed.

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references", In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing In re Lalu, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)). The Examiner in the present case has not met this burden.

Even if the cited art discloses components of the device in issue, case law holds that it is insufficient that the prior art discloses the components of the device in issue, either separately or used in other combination; there must be some teaching, suggestion, or incentive to make the combination made by the inventor. Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 934, 15 USPQ2d 1321, 1323 (Fed. Cir. 1990). Moreover, "obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or

suggestion supporting the combination. Under section 103, teachings of references can be combined ONLY if there is some suggestion or incentive to do so." ACS Hosp. Systems, Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). The Examiner in the present case has not provided any teaching or suggestion from the art supporting the proposed combination.

Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Laskowski, 871 F.2d 115, 10 USPQ2d 1397 (Fed. Cir. 1989); In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984).

Accordingly, the Examiner has improperly used hindsight and Appellant's disclosure to obviate his claimed invention. It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985). Moreover, the CAFC has stated that "One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." In re Fine, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). Accordingly, the Examiner's above-described motivation for combining Aoyama and Hgai to obviate Appellants' Claims 36-39 is in error and cannot be maintained.

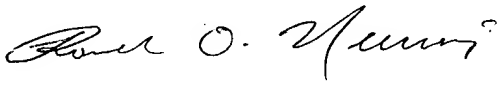
4) Claim 7 is patentable under 35 U.S.C. 103(a) over Aoyama as applied to claim 6 above, and further in view of Ngai et al., EP 0157 306 A3?

Claim 7 further defines the apparatus of Claim 6, wherein said second processor is the main processor of said apparatus. Appellants have previously addressed the deficiencies of using the

Aoyama reference to obviate Claim 6. Moreover, assuming, arguendo, that Ngai et al discloses "the use of a main processor", it fails to overcome the previously identified deficiency of the Aoyama reference. Accordingly the Aoyama reference fails to teach or suggest the further limitation of Claim 7 in combination with the requirements of Claim 6.

For the above reasons, favorable consideration of the appeal of the Final Rejection in the above-referenced application, and its reversal, are respectfully requested.

Respectfully submitted,



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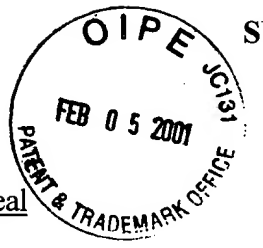

SUBSTITUTE APPENDIX

Claims on Appeal

6. An apparatus, comprising:

a first processor for performing scalar processing, said first processor comprising a core, a program memory and a local memory;

a second processor for performing vector processing, said second processor comprising a core, a program memory and a local memory;

a synchronizing circuit for coupling said core of said first processor to said core of said second processor; and

a memory circuit for coupling said local memory of said first processor to said local memory of said second processor.

7. The apparatus of Claim 6, wherein said second processor is the main processor of said apparatus.

8. The apparatus of Claim 7, wherein said first processor is a microprocessor.

9. The apparatus of Claim 7, wherein said second processor is a digital signal processor "DSP".

10. The apparatus of Claim 6, wherein said program memory of said first processor is ROM memory.

11. The apparatus of Claim 6, wherein said local memory of said first processor is RAM memory.

12. The apparatus of Claim 6, wherein said program memory of said second processor is ROM memory.

13. The apparatus of Claim 6, wherein said local memory of said second processor is RAM memory.

14. The apparatus of Claim 6, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second processor is physically separate from said first and second processors.

15. The apparatus of Claim 6, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second processor is a DPRAM memory.

17. The apparatus of Claim 6, wherein said synchronizing circuit ensures that only one of said first and processors utilizes said memory circuit for coupling said local memory of said first processor to said local memory of said second processor, at any one time. The Asano reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

19. The apparatus of Claim 6, wherein an instruction set is provided to said first processor, comprising at least one field of execution conditions which is intended therefor and comprises at least the following classes of instructions:

integers corresponding to arithmetic and logic operations on integer numbers;

transfer corresponding to the transfer operations between a register in said protocol processor and memory; and

monitoring corresponding to the monitoring of all of the operations modifying the value of an incrementation register in said first processor.

34. The apparatus of Claim 6, wherein said scalar processing encompasses a high-level task which is the monitoring of an application or the management of functioning and tasks which are generally carried out by hard-wired logic which are the protocol processing.

39. An apparatus, comprising:

a main processor comprising a core, a program memory and a local memory;

a protocol processor comprising a core, a program memory and a local memory, said protocol processor being suited to execute tasks to which the main processor is not suited;

a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor; and

one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor.

35. The apparatus of Claim 6, wherein said vector processing includes signal processing tasks generally carried out by a DSP and matrix computation which requires a more powerful structure than that of the DSP and which is generally of the array processor type.

36. An apparatus, comprising:

a first processor comprising a core, a program memory and a local memory;

a second processor comprising a core, a program memory and a local memory;

a synchronizing circuit for coupling said core of said first processor to said core of said second processor; and

one and only one common memory coupling said local memory of said first processor to said local memory of said second processor.

37. An apparatus, comprising:

a main processor comprising a core, a program memory and a local memory;

a protocol processor comprising a core, a program memory and a local memory;

a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor; and

one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor.

38. An apparatus, comprising:

a main processor comprising a core, a program memory and a local memory;

a protocol processor comprising a core, a program memory and a local memory, said protocol processor being suited to execute tasks to which the main processor is not suited;

a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor; and

a common memory coupling said local memory of said main processor to said local memory of said protocol processor.